

Please amend claims 20, 21, 22, 26 and 29 as follows:

20. (Amended) A method of producing a semiconductor integrated circuit device comprising the steps of:

(a) forming bit lines and a first layer wiring over MISFET on a main plane of a semiconductor substrate through a first inter-layer insulating film, forming a second inter-layer insulating film and an electrode-forming insulating film, and etching holes in said electrode-forming insulating film;

(b) forming a metal or a metal compound for providing on an inside of said holes, and then forming cylindrical first electrodes by forming a metal film or a metal compound film covering the inner wall of said holes;

(c) depositing a dielectric capacitance insulating film to cover said first electrodes, and depositing further a first conductor layer and a second conductor layer;

(d) patterning said first and second conductor layers to form second electrodes; and

(e) depositing a third inter-layer insulating film covering said second electrodes, and forming a first connection hole reaching said second electrode and a second connection hole reaching said first layer wiring, by etching, wherein said second conductor layer comprises a tungsten film and said third inter-layer insulating film comprises a silicon oxide film.

21. (Amended) A method of producing a semiconductor integrated circuit device according to claim 20, wherein, after said second conductive layer is etched, said first conductive layer is etched by using said second conductive layer, that is patterned, as a mask.

22. (Amended) A method of producing a semiconductor integrated circuit device including the steps of:

(a) forming first electrodes on a first insulating film formed on a main plane of a semiconductor substrate;

(b) forming a capacitance insulating film over said first electrode;

(c) forming second electrodes over said capacitance insulating film;

(d) forming a second insulating film having an opening for exposing a part of said second electrode, on said second electrode; and

(e) forming a first conductor layer inside said opening; wherein:

the formation step of said second electrode includes the steps of:

(i) forming a first metal layer by a chemical vapor phase growing method containing oxygen over said capacitance insulating film; and

(ii) forming a second metal layer not containing oxygen over said first metal layer, wherein said first conductor layer directly contacts to said second metal layer.

26. (Amended) A method of producing a semiconductor integrated circuit device including the steps of:

(a) forming a plurality of mutually spaced-apart first electrodes over a first insulating film formed on a main plane of a semiconductor substrate;

(b) forming a capacitance insulating film over said first electrodes; and

(c) forming continuous second electrodes with respect to a plurality of said first electrodes, over said capacitance insulating film; wherein:

the formation step of said second electrodes includes the steps of:

(i) forming a first metal layer over said capacitance insulating film;

and

B2
(ii) forming a second metal layer having a greater film thickness than said first metal layer over said first metal layer, and said second metal layer has a lower resistivity than said first metal layer.

29. (Amended) A method of producing a semiconductor integrated circuit device including the steps of:

B3
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(a) forming a plurality of mutually spaced-apart first electrodes over a first insulating film formed on a main plane of a semiconductor substrate;
(b) forming a capacitance insulating film over said first electrodes; and
(c) forming a continuous second electrode with respect to a plurality of said first electrodes, over said capacitance insulating film; wherein:

the formation step of said second electrode includes the steps of:

(i) forming a first metal layer over said capacitance insulating film in such a fashion as to provide within the spaces between said mutually spaced-apart first electrodes; and
(ii) forming said second metal layer over said first metal layer.